The Hybrid Cascode — A General Purpose AGC IF Amplifier

Include this simple, high performance automatic gain control system in your next receiver project.

Wes Hayward, W7ZOI, and Jeff Damm, WA7MLH

Almost every superheterodyne receiver we build has an intermediate frequency (IF)-amplifier with automatic gain control. AGC keeps the receiver output nearly constant for all received signal levels. It also saves our ears should that strong station in the next block decide to join us on our favorite band.

Receiver intermediate frequencies range from 15 kHz up to 100 MHz or higher. A critical requirement for any amplifier that will be part of an AGC controlled IF system is that it have a gain that can be controlled with a voltage. This allows us to reduce gain until the output from our headphones or speaker is at a level we have chosen, and no more.

There are numerous circuits that provide electronic gain control. Many semiconductor manufacturers build integrated circuits with electronic gain control. An excellent AGC system using ICs from Analog Devices was described by Bill Carver, W7AAZ.[1] Special AGC ICs are often expensive, consume considerable current for portable applications, and often have a high noise figure. One of several circuits using discrete components that we investigated is shown in Figure 1, a cascode connection of two junction field effect transistors (JFETs).[2]

A cascode circuit with two devices of the same type is a common form that can be built with bipolar transistors, JFETs, MOSFETs and even vacuum tubes. The cascode connection has several virtues. The first virtue is stability, resulting from a grounded (bypassed) gate in the upper FET in Figure 1. Large output voltages at the J2 drain do not reach the amplifier input at the J1 gate. Most important, this circuit has gain controlled by a voltage. Decreasing the dc voltage on the J2 gate reduces the dc drain voltage on J1, forcing dc current to decrease, thus reducing RF gain. The biasing is set for 10 mA when V_{AGC} is 6 V in this circuit.[3,4]

Use automatic gain control to avoid ear drum damage

The Hybrid Cascode Connection

The circuit of Figure 1 works well when the power supply, V_{DD}, is 12 V or higher. We discovered to our dismay, however, that the performance degrades severely when the power supply voltage drops — a common situation in portable equipment. (Both of us frequently carry portable rigs on backpacking treks into the mountains of the Pacific Northwest.) Lower V_{DD} reduces the maximum gain and severely compromises the gain control characteristics. In an effort to eliminate this problem, we observed that all fundamental virtues of the circuit of Figure 1 are retained if the upper JFET, J2, is replaced with a bipolar transistor. We call this circuit, shown in Figure 2, the hybrid cascode. Setting V_{AGC} to 8.5 V establishes the same conditions on J1 that we had in Figure 1 with a V_{AGC} of 6 V, producing identical maximum gain.

The major difference between the two circuits lies in the dc control. The circuit with two FETs in Figure 1 required a large string of diodes to be in series with the circuit so that the J2 gate voltage could drop far enough to

[1]Notes appear on page 33.

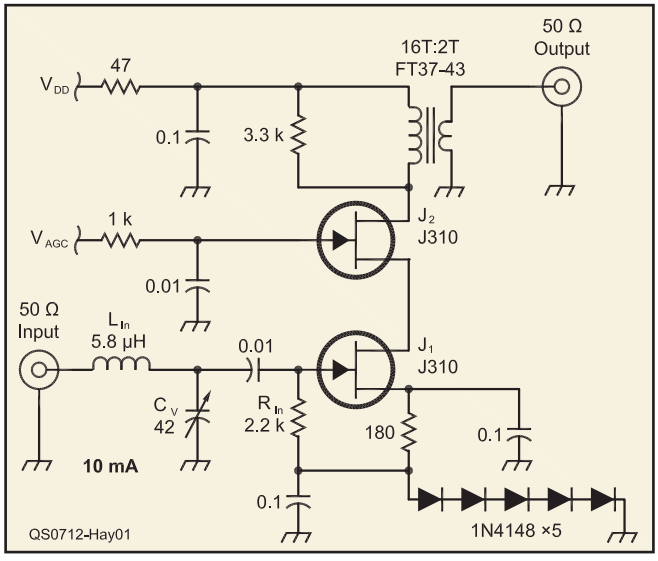

Figure 1 — Traditional JFET cascade IF amplifier. The computer simulated gain of this circuit is 23.5 dB at 9 MHz. Measurements produced similar values.

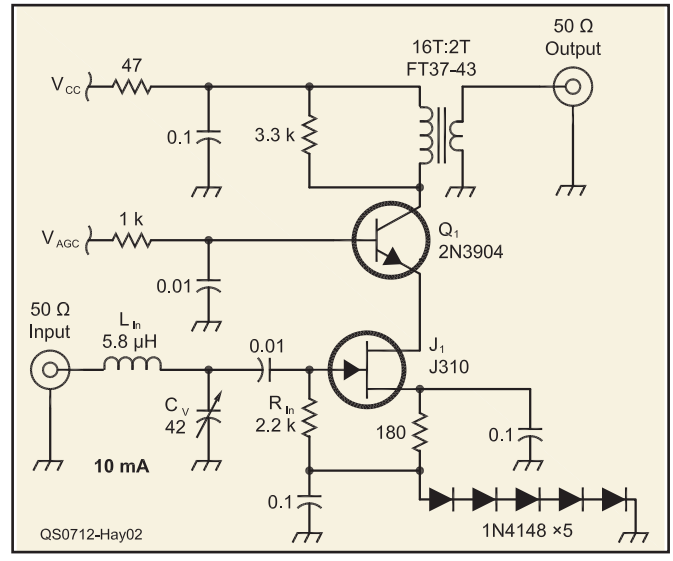

Figure 2 — Hybrid cascode. 9 MHz G_{MAX} of 23.9 dB when V_{AGC} is 8.5 V. Same tuning as Figure 1.

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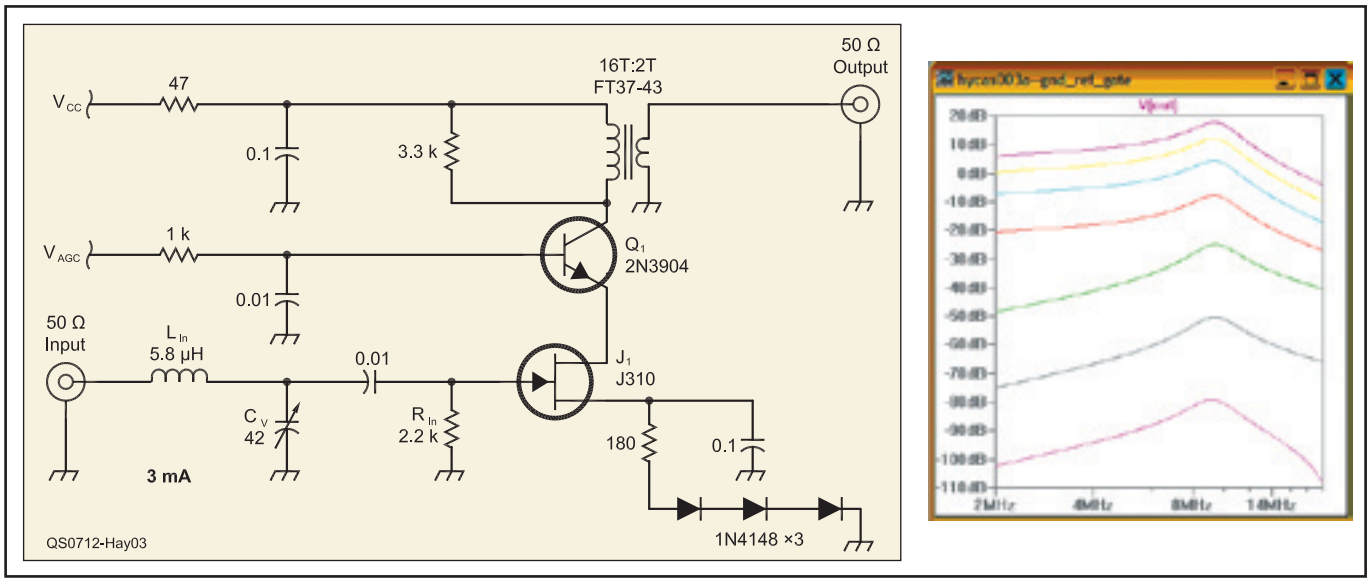


Figure 3 — Ground referenced hybrid cascode amplifier. (Details: V_{AGC} of 4 to 1 in 0.5 V steps, G_{MAX} of 17.7 dB, with virtually no change when V_{CC} drops to 6 V.)

cut off current flow in J1. J1 drain to source voltage and current can be dropped to zero in the hybrid cascode, even without a diode string. This yields a significant power supply margin.

The configuration we ended up using for our later designs is shown in Figure 3. This circuit has lower gain than that of Figure 2, for the maximum current has dropped from 10 to 3 mA. Only three diodes are used with a maximum V_{AGC} of 4 V. The input gate is now ground referenced through R_{IN}. This circuit shows virtually no measured or simulated performance change between V_{CC} of 12 and 6 V. The simulated curves, now in 0.5 V steps in Figure 3, show an extremely wide gain range for a single stage.

The same maximum gain can be achieved with two diodes and a 390 Ω source resistance, or with no diodes and a 750 Ω source resistance. The version of Figure 3 with three diodes and a 180 Ω source resistance provides a greater, and more monotonic, gain control range. Although other FET types can be used, the high I_{DSS} J310 offers a higher maximum gain.

A Receiver IF Amplifier

Figure 4 shows the next step of our design exercise, an amplifier suitable for use in communications receivers. Three hybrid cascode stages are used, offering 100 dB of AGC range. A transformer in the third stage drives a differential pair of PNP transistors, Q7 and Q8. Product detector output is extracted from Q8, while Q7 drives a diode AGC detector. R6 sets the AGC threshold. The value shown yields a dc level of 0.4 V at the detector output with no input signal. Shorting R6 increases the AGC threshold, often producing a more crisp receiver sound. The detected dc drives the base of Q10, which then discharges "memory" capacitor C16. The collector of Q10 also decreases the Q9 base voltage. Q9 is a PNP emitter follower that drives the AGC line which controls the gain of the three cascode amplifiers.

The nominal output level of this amplifier is between –35 and –40 dBm, depending on the value of threshold resistor R6. These levels are optimum to drive a standard diode ring product detector such as a Minicircuits TUF-1 or SBL-1 while keeping distortion low. R3 can be decreased while R4 is increased to drop the level for less robust product detectors.

Three hybrid cascode stages are used, offering 100 dB of AGC range.

The AGC may be turned off with a positive base voltage applied to Q12. A similar positive signal applied to Q11 will mute the amplifier. Diodes from the memory capacitor and the AGC line are routed to a manual gain control.

This amplifier has an overall AGC OFF gain of 55 to 60 dB. This may be altered by using different values for R1 and R2. The gain may also be reduced by using only two cascode stages. The two stage circuit is similar to the IF amplifier used in the popular Progressive Receiver, a design from antiquity that is still being built today.[5] The amplifier input is matched to 50 Ω with an L network (preferred), although a ferrite transformer was used in some of the experimental amplifiers. The values shown in the schematic are for 9 MHz with a match to the 3.3 kΩ gate resistance at Q2. The circuit can be adapted to frequencies throughout the MF and HF spectrum.

We examined the dynamics of this circuit with a pulsed signal generator consisting of a PIN diode modulator following an HP-8640B signal generator.[6] The modulator was driven by a pulse generator. Pulses of 1 mS in length up to –20 dBm in strength occurred once per second. Signals within the IF amplifier were then observed with an oscilloscope. The Q10 saturation resistance confined overshoot to the first 100 µS. These sharp pulses will never reach an IF amplifier that is preceded by a SSB or CW width crystal filter. If necessary, R5 may be increased to slow the attack. AGC recovery time is set by the two 1.5 MΩ resistors charging the memory capacitor and driving the base of Q9.

We included a regulator on the board to provide 9 V to the active circuits. Power supplied to the board down to 11 V is allowed. A low dropout regulator in place of the LM317L would allow an even lower supply voltage.

Construction

The amplifier should be constructed using reasonable RF methods, although we found nothing especially critical in the circuit. The first prototype used "ugly" construction over a ground plane.[7]

A printed circuit board version of the amplifier is shown in Figure 5. This imple-

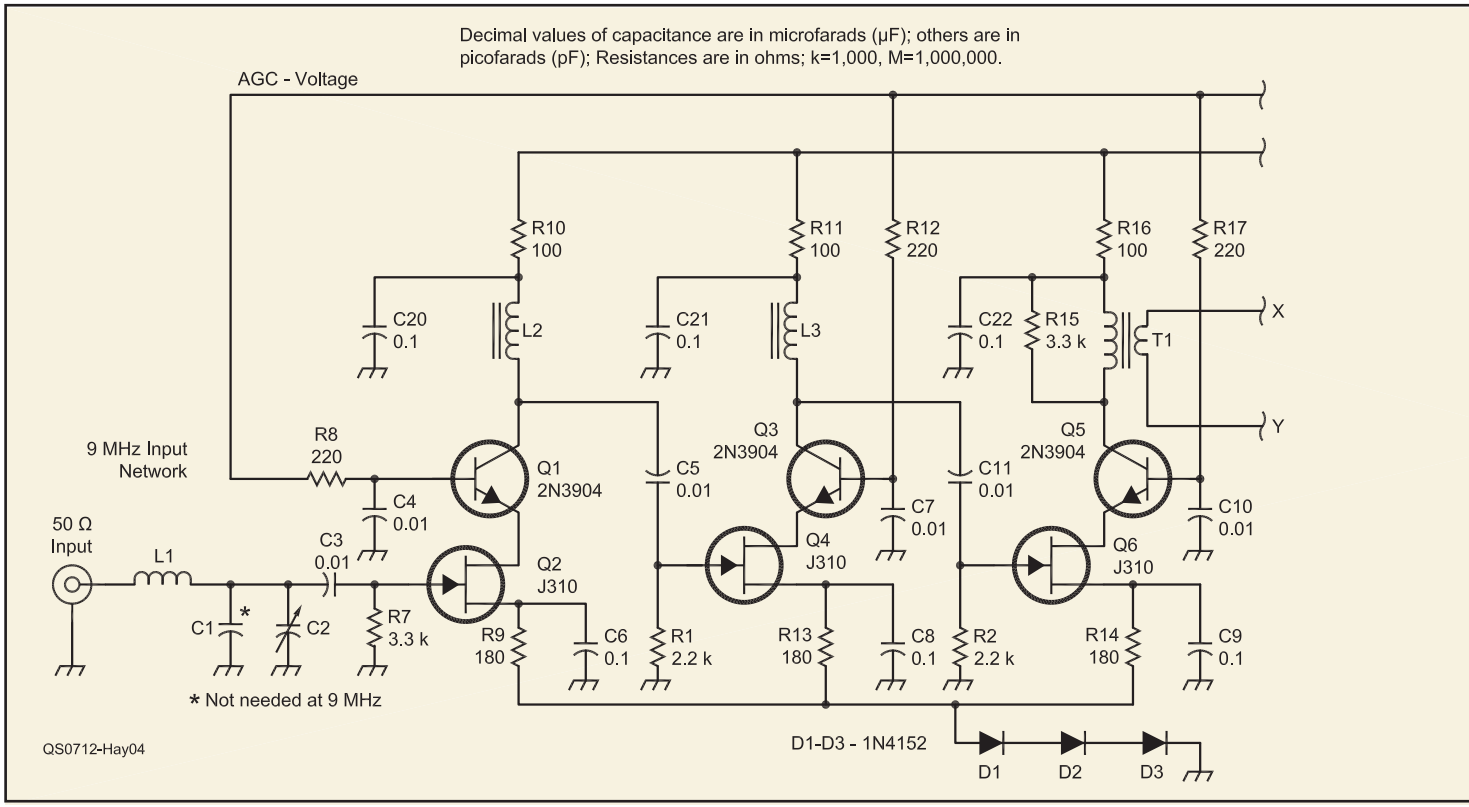


Figure 4 — Schematic diagram and parts list for complete IF amplifier and AGC system for receivers.

C1 — See text. None needed at 9 MHz.
C2 — 65 pF trimmer capacitor.
C3-C5, C7, C10, C11, C15 — 0.01 µF, 50 V ceramic capacitor.
C6, C8, C9, C12-C14, C19-C22 — 0.1 µF, 50 V ceramic capacitor.
C16 — 4.7 µF, 50 V electrolytic capacitor.
C17, C18 — 0.22 µF, 50 V ceramic capacitor.
D1-D5 — 1N4152, 1N4148 or BAV70 small signal diodes.
L1 — For 9 MHz, 7.1 µH inductor. 42 turns 28 gauge enameled wire on a T50-6 toroid core.
L2-L4 — 120 µH SMT inductor, or 16 turns 28 gauge enameled wire on a FB-43-2401 toroid core.
Q1, Q3, Q5, Q10-12 — NPN small signal silicon transistor, 2N3904 or MMBT3904.
Q7-Q9 — PNP small signal silicon transistor 2N3906 or MMBT3906.
R1, R2, R25, R33 — 2.2 kΩ, ¼ W resistor.
R3 — 51 Ω, ¼ W resistor.
R4, R5 — See text.
R6 — 270 Ω, ¼ W resistor.
R7, R15 — 3.3 kΩ, ¼ W resistor.
R8, R12, R17, R34 — 220 Ω, size 1206 for SMT or ¼ W leaded resistor.
R9, R13, R14, R20 — 180 Ω, ¼ W resistor.
R10, R11, R16 — 100 Ω, ¼ W resistor.
R18 — 4.7 kΩ, ¼ W resistor.
R19, R28-R31 — 10 kΩ, ¼ W resistor.
R21, R22 — 680 Ω, ¼ W resistor.
R23 — 47 kΩ, ¼ W resistor.
R24 — 100 kΩ, ¼ W resistor.
R26, R27 — 1.5 MΩ, ¼ W resistor.
R32 — 5 kΩ potentiometer.
R35 — 1 kΩ, ¼ W resistor.
R36 — 330 Ω, ¼ W resistor.
T1 — 16 turns 28 gauge enameled wire on a FB-43-2401 toroid core with output link of 4 turns 22 gauge enameled wire.

mentation used surface mount (SMT) components. The only changes to this circuit from the breadboard were a substitution of SMT inductors at L2, L3 and L4. The inductors used were 120 µH, length 0.3 inches. We measured a Q of 25 for these parts. The diodes were BAV70 in an SOT-23 package. The SMT board layout was generated with the 2.5 × 3.8 inch Miniboard option from Express PCB.[8] The board is double sided with a ground plane covering most of the bottom. Although the printed circuit board is not complete at this writing, we will likely generate a PCB layout for leaded parts as this goes to press.

Further Measurements

The single stage circuit shown in Figure 3 was built and tested for intermodulation distortion and noise figure with a V_{CC} of 12 V and two R_{IN} values. The input network was designed for 2.7 kΩ and was not changed when a higher termination

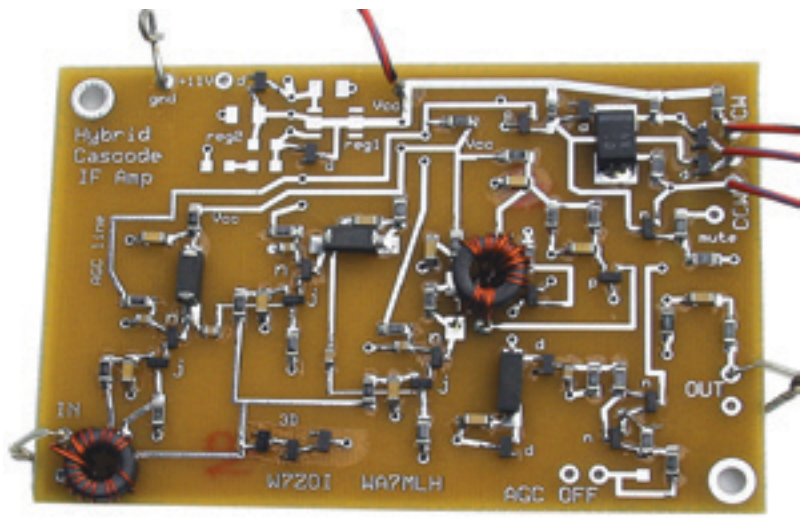
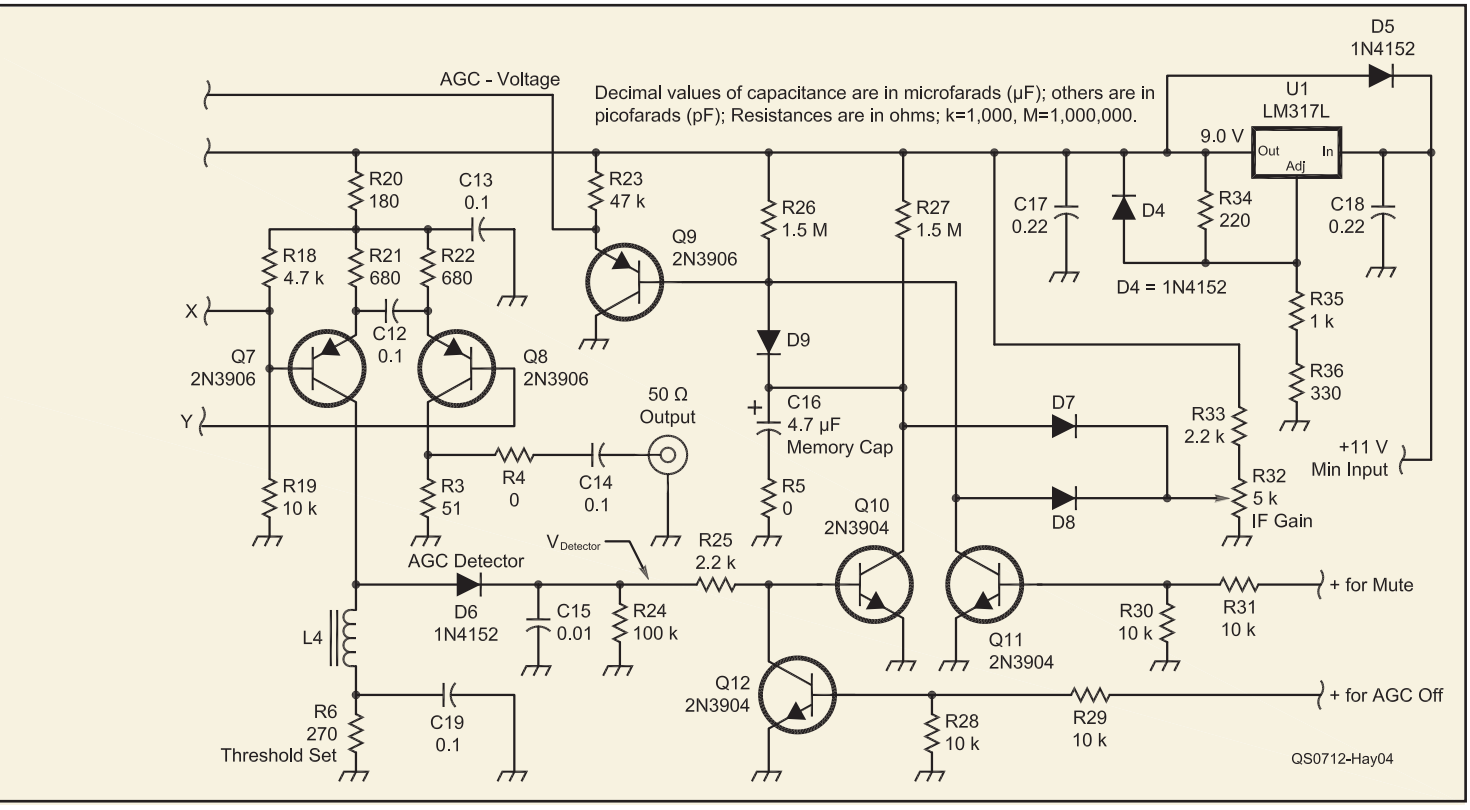


Figure 5 — A printed circuit board version of the IF amplifier using surface mount (SMT) components. The regulator was not installed when the circuit was built and tested with V_{cc} of 9 V.



resistance was applied. We measured a noise figure of 3.9 dB and third order input intercept (IIP3) of +3 dBm when R_{IN} = 2.7 kΩ. This input produced a very good input impedance match. IIP3 increased as gain was reduced while the noise figure remained low until gain became very low. The noise figure dropped to 2 dB when R_{IN} was increased to 22 kΩ, although the input match then became poor. The combination of low noise figure and reasonable IMD make this circuit suitable as an RF amplifier (when really needed) if the bias current is increased to 10 or 15 mA.

Conclusions and Refinements

The hybrid cascode appears to be an excellent general purpose circuit topology for receiver applications. The low noise figure makes it appealing, even compared with high end integrated circuits. The circuit form is easily adapted to other FET and bipolar transistors, making it useful worldwide.

We initially thought that the hybrid cascode circuit with a bipolar and a JFET was new. But we then discovered that it has been in use for a long time, especially in automotive equipment.[9]

The hybrid cascode can be modified by replacing the upper bipolar transistor with a differential NPN pair. This then allows one to apply AGC by current diversion, the scheme used in many popular integrated circuits such as the ubiquitous MC-1350P. Further expansion suggests using this scheme with transformer feedback amplifiers.[10,11] Finally, it appears that the scheme could be expanded to realize low noise, high intercept hybrid mixers.[12,13]

Additional data and information regarding circuit board availability can be found on the W7ZOI Web site.[14]

Acknowledgments

We would like to thank Rick Campbell, KK7B, and Bob Culter, N7FKI, for valuable comments. Thanks also to John Lawson, K5IRK, who built a version of the circuit for one of his receivers.

Notes

[1]W. Carver, "A High-Performance AGC/IF Subsystem", *QST*, May 1996, pp 39-44.
[2]W. Hayward, W7ZOI, R. Campbell, KK7B, and B. Larkin, W7PUA, *Experimental Methods in RF Design*, pp 6.15-6.26. Available from your ARRL dealer or the ARRL Bookstore, ARRL order no. 8799. Telephone 860-594-0355, or toll-free in the US 888-277-5289; **www.arrl.org/shop/**; **pubsales@arrl.org**.
[3]See Note 2, pp 2.5-2.6.
[4]**w7zoi.net/jfet101.pdf**. See JFET tutorial.
[5]W. Hayward and J. Lawson, "A Progressive Communications Receiver," *QST*, Nov 1981, pp 11-16. Also appeared in several editions of *The ARRL Handbook* in the 1980s.
[6]See Note 2, p 7.40.
[7]See Note 2, pp 1.2-1.3.
[8]**www.expresspcb.com/**.
[9]US patent 4,277,757, Richard Kennedy, 1979, assigned to Delco/General Motors.
[10]W. Hayward, *Introduction to RF Design*, ARRL, 1994, pp 215-218. Also see Note 2, p 6.51.
[11]W. Hayward and J. Damm, "The Hybrid Cascode AGC Amplifier," *Proceedings of Four Days in May*, 2007 (QRP ARCI), pp 65-73.
[12]See Note 11.
[13]See Note 11. Also, *Radio Communication Handbook*, RSGB, 8th Edition, 2005, pp 5.4-5.6.
[14]See **w7zoi.net**.

Wes Hayward has been licensed since 1955 as W7ZOI and is now retired from a career in electron-device physics and later, in circuit design. He now devotes his time to some writing, consulting, circuit research and a bit of backpacking and hiking. You can reach Wes at 7700 SW Danielle Ave, Beaverton, OR 97008 or **w7zoi@arrl.net**.

Jeff Damm, WA7MLH, was first licensed in 1968 while in junior high school. He showed up on Wes's doorstep just a few days later. He helped Wes with many breadboarding and construction chores for use in Solid State Design for the Radio Amateur. *His Amateur Radio focus since 1972 has been primarily HF CW/SSB homebrew/design. He has a BSCEE from Oregon State University and has worked the last 26 years in many phases of GaAs digital and RFIC design and product development from VHF through 12 GHz. Jeff is a cofounder of TriQuint Semiconductor. He currently does contract microwave consulting and design of GaAs RFICs. He can be reached at 3384 Winola Ave S, Salem, OR 97302, or* **wa7mlh@neoanderthal.com**.

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