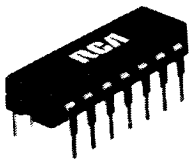
CA1352E



14-Lead Dual-In-Line Plastic Package

H-1517

TV IF Amplifier

With AGC and Keyer Circuit

Features:

- *Gain = 52 dB (typ.)*
- *Gain reduction = 66 dB (min.)*
- *Gated AGC accepts either positive or negative video*
- *Adjustable delay for tuner AGC*

The RCA-CA1352E is a monolithic integrated circuit designed for use as the if amplifier in color or monochrome TV receivers. It incorporates a high-gain gated-AGC system with a range of 66 dB (min.), and the rf AGC delay may be adjusted externally. Separate inputs are provided for positive and negative video; the gated AGC circuit will accept either, depending on the input terminal used.

The CA1352E is supplied in a 14-lead dual-in-line plastic package, and is directly interchangeable with the industry type 1352 in similar packages.

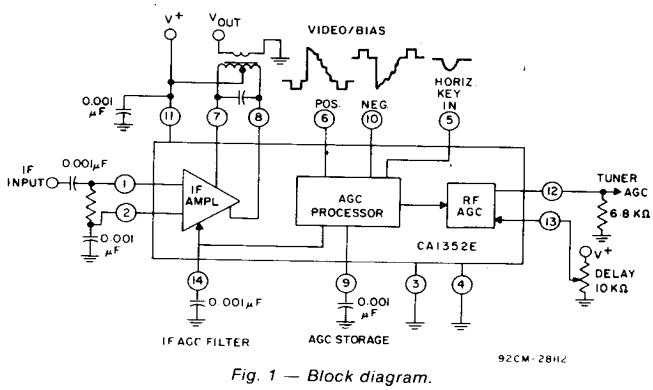


Fig. 1 — Block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

INPUT VOLTAGE (Terminal 1 or 2) ..... 10 V_{p-p}

AGC INPUT VOLTAGE (Terminal 6 or 10) ..... 6 V

HORIZONTAL KEYING VOLTAGE (Terminal 5) ..... +10 to −20 VDC

SUPPLY VOLTAGE:

Between terminals 4 and 11 ..... 18 V

Between terminals 7 or 8 and 4 ..... 18 V

DEVICE DISSIPATION:

Up to T_A = 55° C ..... 750 mW

Above T_A = 55° C ..... derate linearly at 7.9 mW/° C

AMBIENT TEMPERATURE RANGE (T_A)

Operating ..... −40 to +85° C

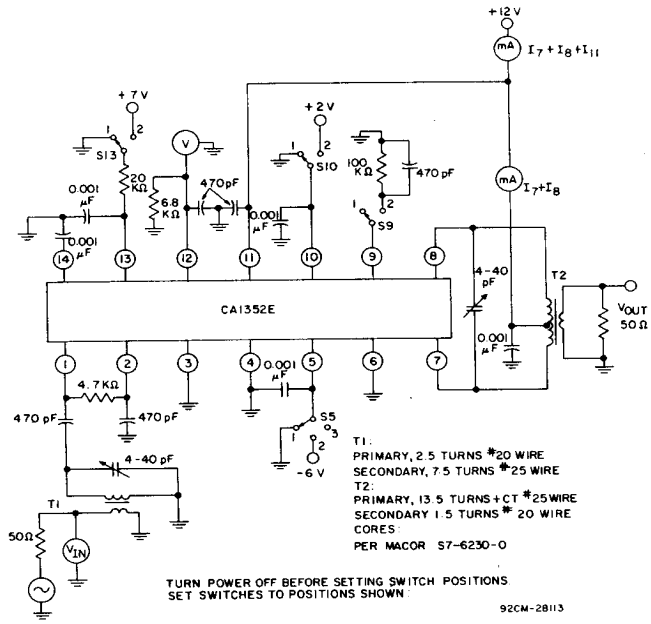
Storage ..... −65 to +150° C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 12 Vdc, f = 45 MHz

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Power Gain	V_{IN} = 100 μV, see Fig.3	43.5	52	–	dB
AGC Range	See Fig.3	66	–	–	dB
Total Current ($I_7 + I_8 + I_{11}$)	No signal, see Fig.3	19	–	35	mA
Output Stage Current ($I_7 + I_8$)		4.6	–	7.4	mA
Tuner AGC Voltage at Terminal 12	No signal	–	–	0.6	V
	Max. signal	6.5	–	–	
Single-Ended Input Capacitance	V_{IN} = 30 mV at 45 MHz	–	10	–	pF
Single-Ended Input Resistance		–	0.9	–	kΩ
Single-Ended Output Capacitance	V_{IN} = 100 mV at 45 MHz	–	2.5	–	pF
Single-Ended Output Resistance	V_{IN} = 100 mV at 45 MHz	–	20	–	kΩ



CHARACTERISTIC	S5	S9	S10	S13	V_I	MEASURE
Power Gain	1	2	1	1	100 μV	V_{OUT} 1
AGC Range	2	1	2	2	Note 1	V_{OUT} 2
Total Current ($I_7 + I_8 + I_{11}$)	1	1	1	1	No Sig.	$I_7 + I_8 + I_{11}$
Output Stage Current ($I_7 + I_8$)	1	1	1	1	No Sig.	$I_7 + I_8$
Tuner AGC Voltage:						
At V_{12} Low	3	1	2	2	100 μV	V_{12} Max.
At V_{12} High	2	1	2	2	100 μV	V_{12} Min.

Note 1: Increase input signal until V_{OUT} 2 = V_{OUT} 1 ($V_I \geq$ 200 mV).

Fig.2 – Test Circuit.

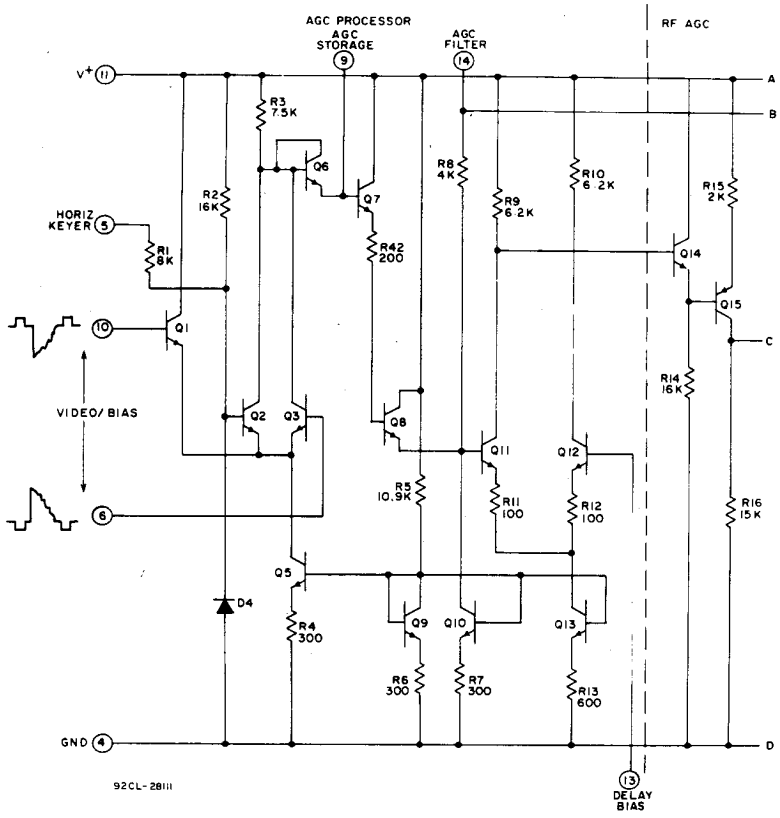


Fig.3 – Schematic diagram.

CIRCUIT DESCRIPTION

As shown in the block diagram, Fig. 1, the CA1352E consists of a high-gain if amplifier (52 dB typ.), an AGC processor which accepts either polarity video signal (approx. 3.5 V_{P-P}), and an rf AGC amplifier with delay circuit. For proper operation the AGC processor requires three inputs:

(1) A negative-going keying pulse of approximately 8 V_{P-P} applied to terminal 5.

(2) A video signal suitably biased.
   a) If a white positive video signal is used, it is applied to terminal 6. The sync tip should be biased at +2 V.
   b) If a white negative video signal is used, it should be applied to terminal 10. The sync tip should be biased to +4.5 V. It is recommended that an additional external resistance of 3.9 kΩ be inserted in series with the key input (terminal 5) when white negative video is used.

(3) The third input to the processor is a dc bias potential.
   a) For white positive video signals the bias is applied to terminal 10. The value of the bias is +1 to +4 Vdc, with a nominal value of +2 V.
   b) For white negative video signals, the bias is applied to terminal 6. The value of the bias is +8 to +1 Vdc, with a nominal value of +4.5 V.

The AGC processor charges the AGC storage capacitor, connected externally to terminal 9, during the keying pulse. The amount of charge is determined by the amplitude of the video signal and the dc bias potential. As shown in the schematic, the current is discharged through Q7. The AGC potential across the external capacitor is applied to the if amplifier and to the AGC delay and control circuits.

The if amplifier consists of a modified cascode-balanced amplifier. The input stages Q21 and Q25 operate at a fixed bias point

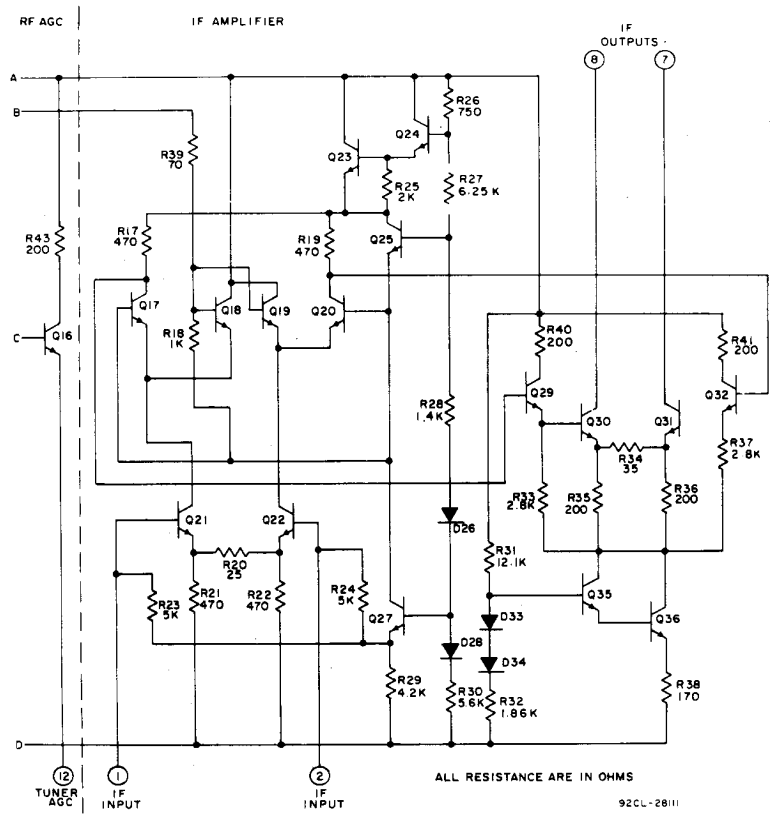


Fig.3 – Schematic diagram.

to reduce the input impedance variations as a function of signal level. At maximum if gain the total collector current of Q21 and Q25 flows through the ac grounded-base transistors Q17 and Q20, respectively. When the signal level at the input increases and the AGC becomes functional, part of the collector currents are diverted to dummy loads Q18 and Q19. The if signal at the collectors of Q17 and Q20 are connected to the balanced output amplifier consisting of Q29 through Q36. The output impedance is held nearly constant because the output stages are operated at a constant current determined by Q36.

The delayed rf AGC voltage at terminal 12 varies from less than 0.6 V with no signal input to greater than 6.5 V at high input-signal conditions.

The tuner AGC threshold point can be changed by the voltage applied to terminal 13. Increasing V13 "delays" the rf AGC so that turn-on occurs with higher input-signal levels.

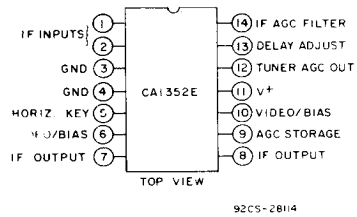


Fig.4 – Terminal assignment.